7. Regarding claim 11, replace the period in the last line with a comma and insert the following new paragraph after the last paragraph: --wherein the second instruction form is a logical subset of the first instruction form, wherein the predecoded instructions of the second instruction form are statically stored in the plurality of buffers, and wherein the predecoded instructions of the second instruction form are control signals generated by a compiler and are not decoded during a runtime of the program.--

8. Regarding claim 13, in line 4, please replace "unit" with --units--.

9. Regarding claim 20, please cancel claim 20.

10. Regarding claim 21, in line 13 (line 2 of the 2nd to last paragraph), replace "form, wherein" with --form, wherein the predecoded instructions of the second instruction form are not decoded during a runtime, and wherein--.

Drawings

11. In response to the application being allowed, formal drawings are now required.

Reasons for Allowance

12. The following is an examiner's statement of reasons for allowance:

Hammond et al., U.S. Patent No. 5,638,525, has taught a system capable of executing two instruction sets, each of which includes a branch instruction to jump to the other instruction set, wherein both sets are stored in the same cache prior to decoding and execution.

Trivedi et al., U.S. Patent No. 6,430,674, has taught a system capable of executing multiple instruction sets, each of which includes a branch to jump to the other instruction set,